REMARKS

Claims 1, 3-9, 11-17, and 19-24 were pending in the present application. Claims 1, 9, and 17 have been amended. Accordingly, claims 1, 3-9, 11-17, and 19-24 remain pending in the present application.

Claims 1, 3, 7, 8, 9, 11, 15-17, 19, and 23-24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ruszczyk (U.S. Patent No. 6,205,150) (hereinafter 'Ruszczyk') in view of Huang et al. (U.S. Patent No. 6,092,137) (hereinafter 'Huang') and in further view of the Free On-Line Dictionary of Computing (hereinafter 'FOLDOC'). The Applicant respectfully traverses this rejection.

Claims 4, 12, and 20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ruszczyk, Huang, and FOLDOC, in further view of Taniguchi (Japanese Patent No. JP 10341240) (hereinafter 'Taniguchi'), and in further view of Olson et al. (U.S. Patent No. 4,677,612) (hereinafter 'Olson'). The Applicant respectfully traverses this rejection.

Claims 5, 13, and 21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ruszczyk, Huang and FOLDOC and in further view of Drottar et al. (U.S. Patent No. 6,343,067) (hereinafter 'Drottar'). The Applicant respectfully traverses this rejection.

Claims 6, 14, and 22 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Ruszczyk, Huang, FOLDOC and Drottar and in further view of Zhang (U.S. Patent No. 6,108,345) (hereinafter 'Zhang'). The Applicant respectfully traverses this rejection.

The Applicant discloses at page 8, lines 1-7

> "During operation, packet I/O bus device 50A and 50B may translate PCI bus transactions into upstream packet transactions that travel in I/O streams and additionally may translate downstream packet transactions into PCI bus transactions. ... **Each I/O stream may be identified by an**

identifier called a Unit ID. It is contemplated that the Unit ID may be part of a packet header or it may be some other designated number of bits in a packet or packets. As used herein, "I/O stream" refers to all packet transactions that contain **the same Unit ID and therefore originate from the same node**." (Emphasis added)

The Applicant also discloses at page 10, lines 8-15

"During operation, a packet transaction may enter upstream router 100. Upstream router 100 may identify the packet by the packet's Unit ID, which may be a five-bit identifier field. Upstream router 100 may assign this packet and all other packets with this same Unit ID to the first available buffer, such as upstream I/O buffer 125A. As each succeeding packet enters upstream router 100 it is examined and assigned to an appropriate buffer. Hence, all packets with the same Unit ID may be stored in the same buffer. Each upstream reorder logic circuit 150A-D may then analyze only those packets contained in the particular buffer that each receives packets from." (Emphasis added)

The Applicant further discloses at page 11, line 24 - page 12, line 4

"each upstream reorder logic circuit 150 of FIG. 2 examines the type of transaction that each packet contains and may reorder the packets based on a set of transaction reordering rules. If upstream reorder logic circuit 150 determines that reordering is necessary, operation proceeds to step 350 of FIG. 3A where upstream reorder logic circuit 150 of FIG. 2 reorders the transactions in upstream I/O buffer 125. Proceeding to step 360 of FIG. 3A, upstream transmitter 175 of FIG. 2 may then transmit each packet upstream. Upstream transmitter 175 may transmit the packets **from each upstream I/O buffer 125 based on a first come first served ordering scheme**. (Emphasis added)

Accordingly, the Applicant's claim 1 recites an apparatus comprising

"a plurality of upstream buffers each configured to store a plurality of upstream packets, wherein each of said plurality of upstream packets contains an associated identifier indicative of a source of each of said plurality of upstream packets; and

a router coupled to each of said plurality of upstream buffers and configured to receive said plurality of packets, and to route each of said plurality of packets to **a given one** of said upstream buffers, depending upon the associated identifier, wherein **a given buffer** of said plurality of upstream buffers **stores only packets having a same source**;

a plurality of upstream reorder logic circuits, wherein each one of said plurality of upstream reorder logic circuits is coupled to a corresponding one of said plurality of upstream buffers and is

configured to determine **a correct order** of transmitting **each of said packets stored** in said corresponding **one** of said plurality of upstream **buffers** based on a set of predetermined criteria, wherein each of said plurality of upstream reorder logic circuits is further configured to **reorder given ones of said packets stored in said corresponding one of said plurality of upstream buffers in response to determining that said order of transmitting is not correct**;

a transmitter unit coupled to said plurality of upstream reorder logic circuits and configured to transmit **one** packet of said plurality of upstream packets stored within said plurality of upstream buffers **dependent upon an order of receipt within said plurality** of upstream buffers." (Emphasis added)

Ruszczyk is directed toward a method of scheduling higher and lower priority data packets, wherein at col. 3, lines 50-64 Ruszczyk discloses

"The method includes a first network device monitoring a first queue with multiple data packets of varying priorities and determining scheduling priorities or transmission deadlines for data packets in the first queue. The multiple data packets provide various class-of-service and quality-of-service connections. After a first network device determines the priority of the data packets, the first network device inserts higher priority data packets into a second queue and lower priority data packets into a third queue. The data packets in the second queue are scheduled for transmission using a first scheduling method as higher priority data packets. The data packets in the third queue are scheduled by a second scheduling method with transmission deadlines as lower priority data packets to be executed after the higher priority data packets." (Emphasis added)

The Examiner acknowledges "Ruszczyk **does not teach** that the packets are routed to a given one of the upstream buffers based on the associated identifier that is indicative of the source of the packet."

Indeed, in addition, Ruszczyk further discloses at col. 6, lines 15-19 "Once a transmission deadline of a lower priority data packet in low priority queue 66 has expired, **a promoter 70 promotes the lower priority data packet to high priority queue 62** whereby the promoted data packet is scheduled by guaranteed scheduling method 64." (Emphasis added)

From the foregoing, it appears that Ruszczyk teaches placing the incoming packets into different queues based upon their respective priorities. Ruszczyk further teaches as long as there are packets in the high priority queue, the high priority packets will be transmitted and if a packet in the low priority queue has a deadline that passes, it will be promoted **(i.e., moved)** to the high priority queue. (Emphasis added)

Thus, not only does **Ruszczyk not teach** that the packets are routed to a given one of the upstream buffers based on the associated identifier that is indicative of the source of the packet, since packets may be moved from one buffer to another, the Applicant asserts that **Ruszczyk does not teach** "...to route each of said plurality of packets to **a given one** of said upstream buffers, depending upon the associated identifier"as recited in Applicant's claim 1. **Ruszczyk** also **does not teach** "wherein **a given buffer** of said plurality of upstream buffers **stores only packets having a same source**," as recited in Applicant's claim 1.

Huang discloses an arbitration device which provides that competing sources have fair access to a shared bus resource while achieving fair and efficient bus utilization. (*See* col. 2, lines 7-13) Huang teaches using a priority-weighted value to arbitrate between competing sources.

The FOLDOC reference merely teaches a use of FIFOs in buffering schemes (e.g., first in, first out) for sending and receiving data. The Applicants find no particular relevance to this reference, since in the Applicant's invention, the data may be reordered within a given buffer depending on not only arrival time but also packet transaction type, thus the buffers need not be FIFOs. Furthermore, Applicant's claim does not claim transmitting packets based on order of receipt in a given buffer. Applicant claims "transmit **one** packet of said plurality of upstream packets stored within said plurality of upstream buffers **dependent upon an order of receipt within said plurality** of upstream buffers." Thus it is clear that the Applicant's transmitter selects across all buffers, after the reorder logic has reordered the packets within each buffer, according to such criteria

as arrival time and packet transaction type, for example. The FOLDOC reference does not teach this.

However, the Applicant asserts that even if, *arguendo*, one were to combine Ruszczyk with Huang and FOLDOC, one would not obtain the invention as recited in the Applicant's claim 1. Specifically, since in the teachings of Ruszczyk, the sorted packets may be moved from one queue to another based on their priority, (which the Examiner asserts is analogous to packet source) the Applicant's invention would be rendered ineffective or inoperable. Thus, the Applicant respectfully submits that the references are not properly combinable and that Ruszczyk appears to teach away from the Applicant's invention since packets may be moved from one buffer to another (which, as noted above, would render he Applicant's invention ineffective or inoperable).

In addition to Applicant's assertion that the references are not properly combinable, the Applicant further disagrees with the Examiner's assertion of the motivation to combine the references. The Applicant cannot find any motivation to combine the references as the Examiner has suggested, either explicitly or inherently in any of the references. The Examiner asserts that one skilled in the art would be motivated to combine the teaching of Huang with the teaching of Ruszczyk. Applicant respectfully disagrees. More particularly, since Ruszczyk already solves the problem of prioritizing of packets, Applicant can fond no motivation to combine Huang with Ruszczyk.

The Applicant respectfully submits that neither Ruszczyk, Huang nor FOLDOC, taken singly or in combination, teach or suggest the combination of features recited in the applicant's claim 1. Accordingly, the Applicant submits that claim 1, along with its dependent claims, patentably distinguishes over Ruszczyk in view of Huang and FOLDOC, over Ruszczyk, Huang, FOLDOC, and in further view of Olson and Taniguchi, and over Ruszczyk, Huang, FOLDOC and in further view of Drottar and over Ruszczyk, Huang, FOLDOC, and in further view of Zhang for the reasons given above.

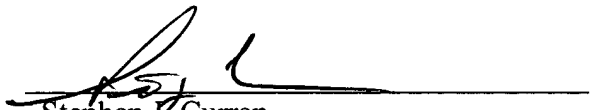
Likewise, neither Ruszczyk, Huang nor FOLDOC, taken singly or in combination, teach or suggest the combination of features recited in Applicant's claims 9 and 17. Thus, claims 9 and 17, along with their respective dependent claims, are believed to patentably distinguish over Ruszczyk in view of Huang and FOLDOC, over Ruszczyk, Huang, FOLDOC, and in further view of Olson and Taniguchi, and over Ruszczyk, Huang, FOLDOC and in further view of Drottar and over Ruszczyk, Huang, FOLDOC, and in further view of Zhang for at least the reasons given above.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any fees are due, the Commissioner is authorized to charge said fees to Meyertons, Hood, Kivlin, Kowert, & Goetzel, P.C. Deposit Account No. 501505/5500-66800/SJC.

Respectfully submitted,



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